A 28-nm CMOS 76–81-GHz Power Amplifier for Automotive Radar Applications

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Abstract — A 28-nm 3-stage single-ended CMOS 76–81-GHz power amplifier (PA) is presented to meet the extended temperature range of 125 °C and quality requirement for Automotive radar sensors. The proposed PA has single-ended input and output ports to minimize pin count, current consumption, die size and remove the need for off or on chip baluns. The three stages are implemented as common-source stages. A combination of Coplanar waveguide (CPW) and inductors are used for impedance matching and impedance transformation purposes for best compromise between the conflicting products die size and performance requirements. At 125 °C ambient temperature, the PA achieves linear power gain of 17 dB, with saturated output power of 12 dBm and output 1-dB compression point of 7.5 dBm, and peak PAE of over 13%, translating to less than 100 mW of power drain. The output power varies by less than 2 dB across the combined frequency band of 76–81 GHz and ambient temperature range of 25 °C to 125 °C. The PA occupies a die area of 590 μm × 300 μm. To the best of the authors’ knowledge, the developed PA shows the best output power, PAE and die size performance, with best frequency and temperature stability for extended temperature range of 125 °C among 76–81-GHz CMOS automotive PA’s reported to date, achieving performances so far seen from high-end SiGe PA’s, yet with much lower power consumption.

Index Terms — Automotive radars, ADAS, CMOS, autonomous driving, mmWave, power amplifier, transceiver.

I. INTRODUCTION

Automotive radar systems operating in 76–81 GHz Band have gained high interests recently due to their use in Advanced Driver Assistance Systems (ADAS) and their potential use in autonomous driving applications. The silicon content of an Auto Radar system can be roughly divided between the front end sensor consisting of the mmWave transceiver chip and the associated functions plus the MCU + DSP + Memory chip(s), with the latter developed in deep sub-micron CMOS. Radar sensor front end transceiver chips have been developed primarily by using SiGe BiCMOS [1-2] technologies. Design of millimeter-wave automotive transceiver ICs using advanced deep sub-micron CMOS technologies is challenging due to the stringent requirements for achieving (1) high output power requirements in presence of lower reported $f_{\text{max}}$ for CMOS technologies, and (2) extended temperature range (125 °C) and very stringent reliability and safety requirements mandated for automotive applications which further accentuates the above mentioned shortcomings. This has led to somehow slower introduction of CMOS Radar chipsets into market. However the increasing digital content of Radar sensors and demand for higher levels of integration and pressure for lower cost has necessitated the introduction of deep sub-micron CMOS Radar front end ICs into markets. The commercially available automotive radar transmitter ICs require output power of > 10 dBm single-ended across the frequency (76–81GHz) and temperature (-40 °C to 125 °C) range, with higher temperature corner being most challenging. It is shown that CMOS PA’s reported to date [4-7] have not achieved such a high output power combined with small die size and high power added efficiency (PAE) at 125 °C. In this paper, we present a 28-nm CMOS highly efficient PA satisfying these requirements up to 125 °C ambient.

II. DESIGN OF THE PROPOSED PA

Fig. 1 shows a simplified schematic of the proposed PA (excluding on-chip bypass capacitors). All three stages are designed based on common-source topology and on-chip bypass capacitors. The three stages are implemented as common-source stages. A combination of Coplanar waveguide (CPW) and inductors are used for impedance matching and impedance transformation purposes for best compromise between the conflicting products die size and performance requirements. At 125 °C ambient temperature, the PA achieves linear power gain of 17 dB, with saturated output power of 12 dBm and output 1-dB compression point of 7.5 dBm, and peak PAE of over 13%, translating to less than 100 mW of power drain. The output power varies by less than 2 dB across the combined frequency band of 76–81 GHz and ambient temperature range of 25 °C to 125 °C. The PA occupies a die area of 590 μm × 300 μm. To the best of the authors’ knowledge, the developed PA shows the best output power, PAE and die size performance, with best frequency and temperature stability for extended temperature range of 125 °C among 76–81-GHz CMOS automotive PA’s reported to date, achieving performances so far seen from high-end SiGe PA’s, yet with much lower power consumption.

Fig. 1. Schematic of the proposed 76–81-GHz PA.
The PA has a single-ended input with ESD protection inductor implemented as $CPW_{in}$, matching $CPW$, and capacitor $C$. The output of first stage then matched to second stage with $CPW$ and is further amplified in second cascade stage $M_2$ and $CPW$. The final stage, $M_3$, amplifies the signal to the right level and delivers the power to the antenna of 50\,$\Omega$ impedance. The value of inductance $L_1$, $CPW_6$, and $C_4$ are carefully determined through load-pull simulation for optimum power transfer to the external antenna load. Each stage has its own gate bias voltage ($V_{b1}$, $V_{b2}$, and $V_{b3}$). Since the required inductance for the final stage is significantly higher than that in the previous two stages, it was implemented using a “half turn” inductor instead of CPW to save area. All inductors and CPWs are designed and simulated using a full 3D EM simulation tool. This design methodology has led to relatively good correlation between simulation and measured data. At 80 GHz, the simulated inductor’s Q is ~13, and the simulated insertion loss of the CPWs is ~0.9 dB/mm.

### III. Fabrication and Measurement Results

The proposed PA was fabricated in a 28-nm CMOS process with 10 metal layers. Its die photograph is shown in Fig. 2. The PA core occupies a physical die area of 590 $\mu$m $\times$ 300 $\mu$m. The PA was measured with on-wafer probing. The measured vs simulated output power, gain and PAE, all at 125 \,°C, with a 0.95-V power supply and all gate bias set to 0.6V, are presented in Fig. 3 at bottom (81GHz), mid (78GHz) and top (76GHz) of the frequency band. Fig. 4 shows the measured and simulated PA small signal S- parameters under the same conditions.

Fig. 2. Die photograph of the developed PA.

Fig. 3. Measured vs simulated output power, gain, and PAE at 125 \,°C, at (a) 76GHz, (b) 78GHz, and (c) 81GHz, respectively.
IV. CONCLUSION

A 28-nm highly efficient PA has been developed employing three common-source stages. CPWs are used for input, intermediate match and load impedance for all stages except for the final stage where a single “half turn” inductor is used. All inductors and CPWs are designed and simulated using a 3-D EM simulation tool. This has led to relatively good correlation between measurement and simulated data for the first silicon. Table I summaries performance of the state-of-the-arts mmWave PA’s. To the best of the authors’ knowledge, the developed PA shows the highest saturated output power at 125 °C and achieved comparable PAE and die size performance to that of [7], with best frequency and temperature stability for extended temperature range of 125 °C among 76–81-GHz CMOS automotive PA’s reported to date. It also achieved performances so far seen from high-end SiGe PA’s, yet with much lower power consumption.

REFERENCES


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(1) Probe pads included.

Table I: Performance Comparison of the State-of-the-Arts mmWave PA’s

Fig. 4. Measured vs simulated PA S-parameters.