A 28-nm CMOS 40-GHz High-Resolution Digitally Controlled Oscillator for Automotive Radar Applications

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Abstract — We present the first millimeter-wave digitally controlled oscillator (DCO) in a 28-nm CMOS technology. This DCO is developed as an integral part of all-digital phase-locked loop for automotive radar applications. The DCO achieves a tuning range of 3.6 GHz (39.3–42.9 GHz) with a fine frequency resolution less than 1 MHz and phase noise of -99.5 dBc/Hz at 1-MHz offset at 39.3 GHz. The DCO occupies 0.08 mm² and consumes 10.5 mW. Impacts on DCO design from closely filled dummies to meet extremely stringent local density rules in the 28-nm CMOS process, which has not been investigated before, are also discussed.

Index Terms — All-digital PLL (ADPLL), CMOS, digitally controlled oscillator (DCO), density rules, mm-wave.

I. INTRODUCTION

All-digital phase-locked loop (ADPLL) has received much interest for its applications in various millimeter-wave (mm-Wave) systems, as CMOS technologies migrate into deep sub-micron region [1]-[5]. Compared with conventional analog-intensive PLLs, all-digital PLLs are superior due to their higher integration level and flexibility and lower power consumption. As an integral part of ADPLLs, DCOs are required to have a wide tuning range, high resolution, low phase noise, and linear tunability is typically desired. To this end, multiple mm-Wave CMOS DCOs have been designed in [6]-[8]. In this paper, we report the first mm-Wave DCO in a 28-nm CMOS technology for automotive radar applications. The use of 28-nm CMOS technology poses new challenges on DCO design. Supply voltages are further reduced to 0.9 V in order to not to damage the devices, resulting in a lower voltage swing and higher achievable phase noise. In addition, very stringent local density rules, even required to meet in small inductor and capacitor areas, add an extra difficulty to attain a large incremental or precise attofarad capacitance. As such, the way to layout a DCO and necessary dummy tiles become essential to obtain those desired performance.

II. DCO DESIGN

The proposed DCO schematic is shown in Fig. 1. This DCO uses a pair of cross-coupled transistors $M_2$ and $M_3$ to generate a negative $G_m$, whose value is controlled through a NMOS current mirror $M_0$ and $M_1$ and an input reference current $I_{ref}$. Large sizing is applied to $M_0$ and $M_1$ for a low flicker noise. $M_0$ has a length of 0.24-$\mu$m and a total width of 180-$\mu$m with 2-$\mu$m fingers, and $M_1$ is ten multiples of $M_0$. In addition, both of $M_1$ and $M_2$ have a length of 28 $\mu$m and a total width of 28 $\mu$m with 1-$\mu$m fingers for a low phase noise. The drains of $M_2$ and $M_1$ are connected to a tunable $LC$ tank which comprises a transformer and three capacitor banks. The prime and secondary inductor of the transformer are 80 $\mu$H and 75 $\mu$H respectively, and both of their $Q$-factors are 16. The low coupling coefficient of $k$ equal to 0.34 is chosen in order to alleviate minimum incremental capacitance of less than 10 aF that is required by 1-MHz or higher resolution. Three capacitor banks, $CB$, $MB$, and $FB$, are designed respectively for coarse, medium, and fine frequency tuning, in which 15 capacitors constitute $CB$, 14 capacitors form $MB$, and 30 capacitors form $FB$. As seen in the inset of Fig. 1, each of these capacitors is physically implemented by two parallel metal strips. Particularly, all of their top metals use the AP layer to reduce resistance loss, and for the bottom metal strips, $CB$ uses the M10 layer, the $MB$ and $FB$ use the M9 layer. To tune the frequency, each of $\pi$-switches is driven by input digital signals through an SPI interface and thermometer decoders to toggle capacitor values. $M_{p}$, $M_{n}$, and $M_{d}$ in the switch that controls $CB$ all have a length of 28 $\mu$m and total width of 8 $\mu$m, and that controls $MB$ and $FB$ have the same length but a total width of 1 $\mu$m. Further, the output of the DCO is ac-coupled with a differential common-source buffer amplifier that
followed by a balun that transforms differential signals to the single-end to drive a 50-Ω load for measurement.

**III. RESULTS AND DISCUSSIONS**

The DCO is fabricated in a 28-nm bulk CMOS technology and its die photograph is shown in Fig. 2. The DCO core occupies a physical die area of 170 μm × 470 μm that excludes pads, bias lines, and digital interface circuitry. The DCO uses a 1-V supply voltage and consumes the total power of 10.5 mW (DCO core only).

The DCO was measured with on-wafer probing, and the measured coarse and medium tuned frequencies are shown in Fig. 3, where the y-axis is 16 coarse-band frequencies tuned by \( CB \) and the x-axis is 15 medium-band frequencies tuned by \( MB \). The DCO achieves a tuning range of 39.3 GHz to 42.9 GHz, i.e. 3.6-GHz bandwidth.

As mentioned earlier, the 28-nm CMOS process has a stringent requirement on local metal densities of \( M_1 \) to \( M_{10} \) layers. The used transformers and capacitors without dummy fills are simulated with an EM simulator HFSS. To evaluate the impact of extensive dummy metal fills around the DCO, we compared the measured and simulated frequency tuning steps for each capacitor tuning bank as shown in Fig. 4. Fig. 4(a) shows the \( CB \)-tuned frequencies, from which we can see that the measured frequency shift up by 0.3–0.68 GHz and the tuning step matches very well with the discrepancy less than 15 MHz. The shift in frequencies is probably resulted from the reduced inductance of \( L_{\text{CI}} \) after filling dummies. As shown in Fig. 4(b) and (c), the averaged \( MB \) and \( FB \) tuning steps in measurement are close to those of simulations except fluctuation that is attributable to both parasitic coupling and fabrication mismatch. It is also observed that the achieved resolution is less than 1 MHz.

Phase noise is measured at 39.3 GHz and 42.9 GHz with a spectrum analyzer as shown in Fig. 5. Fig. 6 shows the measured phase noise versus input reference current varying from 0.6 mA to 1.4 mA. An optimal phase noise is attained at the bias current of 10.5 mA with 1-mA reference from an external source. With this bias condition, the phase noise is –99.5 dBc/Hz and –94 dBc/Hz at 1-MHz offset from 39.3 GHz and of 42.9 GHz of oscillation frequencies,
respectively. Two little noise humps occurring at 2-MHz and 8-MHz offset are likely produced by the reference current. The measured output power is about 1-to-3 dBm across the entire tuning range and S11 is below -10 dB over 36–54 GHz. Table I summarizes and compares the DCO performances. The proposed 28-nm DCO has the best resolution and a comparable FoM as compared to other CMOS technologies.

IV. CONCLUSION

A 28-nm CMOS 39.3–42.9-GHz DCO with frequency resolution less than 1 MHz is developed. The DCO exhibits phase noise between −99.5 dBC/Hz and −94 dBC/Hz over the whole frequency tuning range. It is also demonstrated that the measured frequencies are in good agreement with the simulation even at presence of closely filled dummy metals. The developed mm-Wave DCO can be suitably integrated with ADPLLs for automotive radar applications.

![Fig. 5](image1.png)

Fig. 5. Measured phase noise at the frequencies of 39.3 GHz and 42.9 GHz.

![Fig. 6](image2.png)

Fig. 6. Measured phase noise at 100-kHz and 1-MHz offset frequencies vs. reference current.

TABLE I

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<td>Phase Noise @ 1MHz (dBC/Hz)</td>
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<td>176</td>
<td>178</td>
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a. Only includes DCO core.
b. FoM=20log(fo/Δf)-PN-10log(PDC/1 mW)

REFERENCES